

MicroNote 111

Parasitic Lead Inductance on Transient Voltage Suppressors and Subsequent Overshoot Effects

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Faraday's law of induction states that when current flow through an inductor abruptly stops, a voltage drop is developed across that inductor. This applies to any inductive component, which may be as large as a power distribution transformer or as small as a seemingly insignificant component lead wire. For both, the same relationship applies.

$$v(t) = -L (di/dt)$$

A voltage is developed across the inductive load proportional to the time rate of change in current flow.

This phenomenon can produce "voltage over-shoot", or ineffective clamping of a silicon transient voltage suppressor (TVS), on the leading edge of an incident voltage spike when sufficient parasitic lead inductance is present in the protective loop. Overshoot is illustrated with a comparative circuit in Figure 1 (see page 1).

Figure 1: Voltage Overshoot

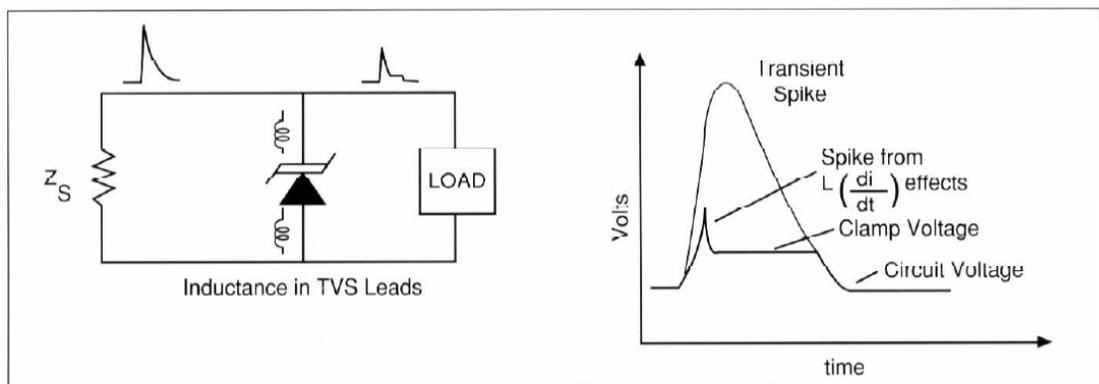
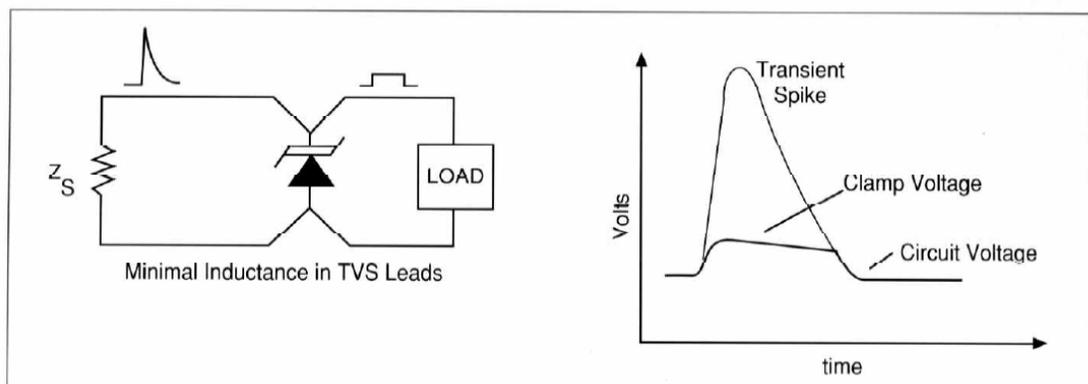


Figure 1. Voltage Overshoot

Figure 2: Optimized Protection



Inadequate protection can result if the overshoot is above the failure or upset level of the protected device. Eliminating the parasitic lead inductance in a protective application produces virtually no overshoot and provides optimum protection, as illustrated in the associated circuit in [Figure 2 \(see page 1\)](#).

The absence of L (di/dt) effects optimizes the protection features of a TVS.

For induced lightning and inductive load spikes, transient rise-times are usually slow in the microsecond range. Hence, TVS lead lengths are not a significant factor unless surge currents are very high (e.g., 100 A or more).

The fast rise-times of electrostatic discharge (ESD) in the subnanosecond range can be a major influence on L (di/dt) effects even at low currents of a few A. High-altitude electromagnetic pulse (HEMP) will produce similar effects with its nanosecond rise-times.

Axial lead devices have approximately 10 nH of lead inductance for normal mount configurations while surface mount devices have 4 nH. MELF packages contribute the least inductance of about 1 nH, which makes them an ideal configuration for ESD protection. Circuit board traces are also part of the protection loop, so layout must not add additional inductance.

When stacking devices in series for higher current capability, as described in [MicroNote 112](#), it is necessary to keep interconnecting wires as short as possible to minimize parasitic lead inductance. For some applications, the writers have found it necessary to parallel some segments to reduce the number of series elements to enhance performance.

There will always be a certain amount of parasitic lead length in a TVS protection circuit, but an effective design should maximize performance by minimizing inductive voltage overshoot to an insignificant level.

Support

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