

## QFN Paddle Landing Layout Pattern Recommendations

Microsemi products achieve high levels of performance in part due to a carefully designed interface between external connectors and internal components. As a result, specific handling precautions must be observed for device reliability and optimum performance.

### Scope

This document outlines the basic QFN (Quad Flatpack No-Leads) ground paddle solder layout landing pattern for Microsemi's Surface Mount Technology (SMT) electronics components.

### Introduction

Microsemi designs and manufactures driver amplifiers, phase frequency detectors, dividers, and prescalers. Many of these driver amplifiers, detectors, dividers, and prescalers are packaged in SMT QFN packaging. The QFN packaging has smaller geometries, better grounding, and improved thermal properties. See Figure 1 for examples of QFN package.

The QFN packages typically have a center metal pad (a.k.a., ground paddle or paddle) on the underside of the part. It's used for grounding and for heat transfer to the printed circuit board (PCB). Soldering this center metal pad to the PCB is usually a challenge for most users. This paper will provide one of the many stencil pattern configurations available to optimize the solder connection between the components' ground paddle and the PCB.

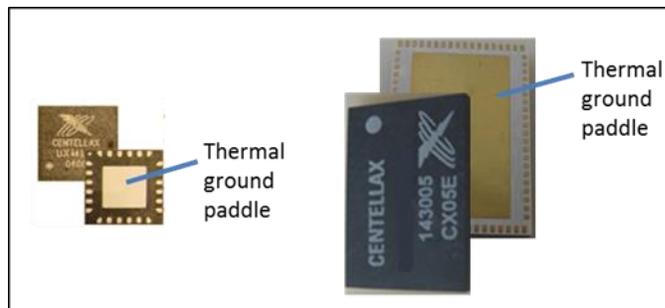


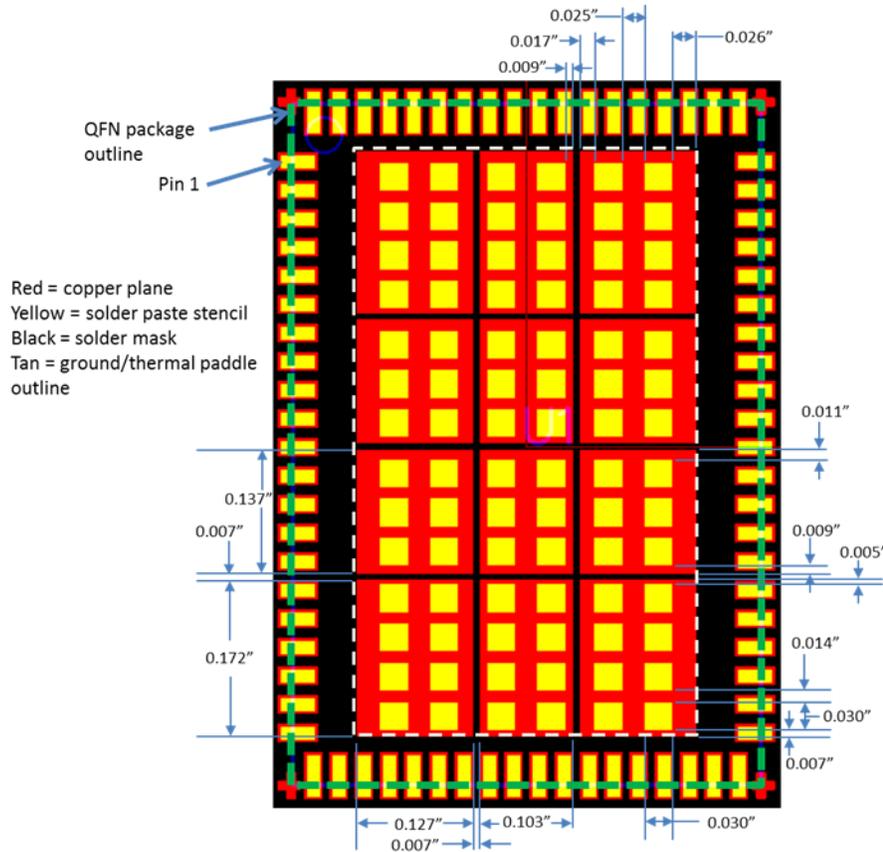
Figure 1: Examples of QFN package

### Solder Stencil Design for the Ground Paddle

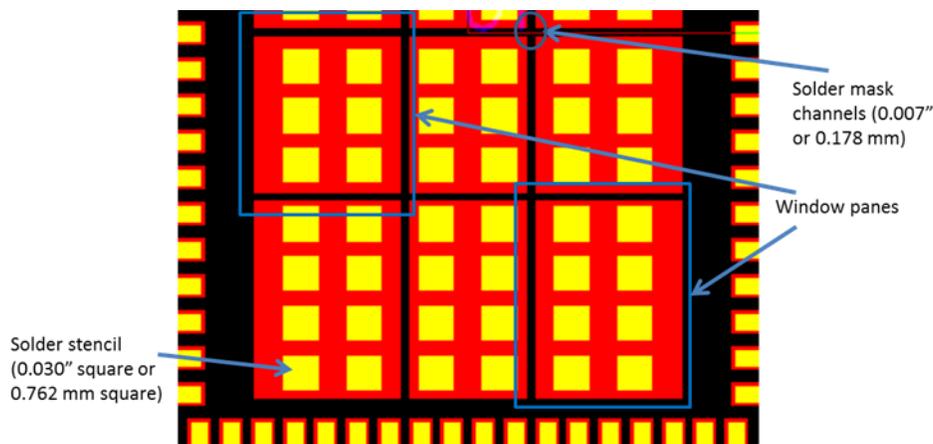
For maximum package thermal dissipation, it's recommended that the QFN package's ground paddle be soldered directly to the user's PCB. A large stencil opening layout design may result in a poor solder connection between the paddle and the PCB. Typically with a single large opening solder stencil design for the paddle, most of the solder will likely adhere and gather to one section of the paddle causing the solder to be non-uniform across the total paddle surface area.

For optimum solder across the paddle surface area, it's recommended to subdivide the solder stencil aperture opening into many window panes or segments for the ground paddle on the PCB as shown in Figure 2. This includes, for example, maintaining a 0.007 inches (or 0.178 mm) channel opening between subdivided window panes, with solder mask material. Also having a 0.003 inches (or 0.076 mm) tall solder mask, and with about 0.006 inches (or about 0.152 mm) height of solder paste stencil to keep the component up high enough above the window pane solder mask allowing for the flux volatile gas to escape during solder reflow, thus minimizing voids. The base idea is to distribute a lower quantity of solder over a broader area, reducing the chance of high-centering and other problems associated with large solder paste areas. See Figure 3 for a close-up view of the window panes.

Package footprints pattern for their associated Microsemi's components in CAD format is available upon request, please contact Microsemi.



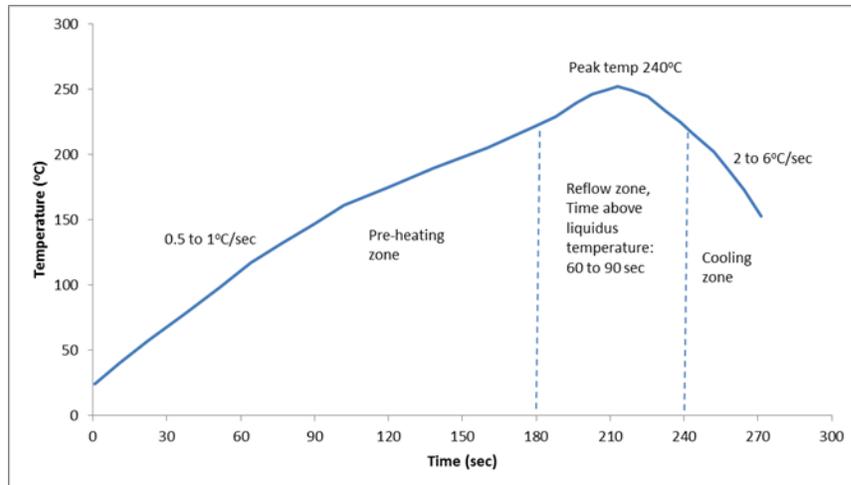
**Figure 2:** Example of PCB solder stencil pattern for the paddle of a 13x19 mm driver amplifier



**Figure 3:** Close-up view of the ground paddle windowpane pattern for exposed stencil pad opening

### Solder Reflow Profile

Microsemi recommends no-clean, Type 3 or Type 4 solder paste to be used for mounting QFN packages. Reflow profile and peak temperature have a strong influence on void formation. Microsemi recommends that the users follow the profile recommendation of the solder paste suppliers. As reference, figure 4 shows an example of a lead-free solder reflow profile.



**Figure 4:** Example of lead-free solder reflow profile

For additional reference information on solder reflow profile, see Microsemi's Application Note AN08 - Surface-mount QFN Package - Handling and Assembly.

**Note do not exceed maximum soldering reflow peak temperature of 250 °C.**

The above application note can be found at Microsemi's websites:

- 1) [www.microsemi.com/products/optical-solutions/optical-literature](http://www.microsemi.com/products/optical-solutions/optical-literature).



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