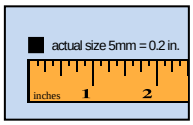
Microsemi's High-Performance 5x5mm Clock Synthesis, Frequency Conversion and Jitter Attenuator Products

Versatile, Easy-to-Use Solutions for a Wide Variety of Timing Challenges



Introduction

Electronic equipment designers continually pack more functionality into smaller systems. As the component count increases in these systems, the number of clock signals needed by processors, NPUs, ASICs, FPGAs, ASSPs and PHYs also grows. Some clock signals must be synchronized to reference clock signals. Other clock signals can be synthesized directly from crystals or crystal oscillators. The clock frequencies required range from 1Hz to more than 1GHz, and clock signal formats and amplitudes vary as well. In some cases the clock ICs are required to monitor their input clocks and have sophisticated switching behavior.

To address these complex requirements, simplify the design of clock networks, and meet cost constraints, equipment designers need small, versatile, high-performance clock ICs they can learn easily and reuse many times. Microsemi's family of 5x5mm clock multipliers and jitter attenuators are general-purpose products that meet the needs of electronic equipment designers. The four products in this family are pin-compatible, register-compatible, and collectively give designers options ranging from simple frequency synthesis to clock multiplication and frequency conversion.

This document presents several common clocking challenges to be solved in today's systems. For each scenario it also shows how one of these Microsemi products meets the requirements for that design. These scenarios show the flexibility and utility of this family of high-performance devices.

Frequency Synthesis

Many clock signals in electronic systems have no requirement to be synchronized with any other clock signal. These signals, therefore, can be *synthesized* (created, generated) in any way that is convenient. Historically system designers have selected one or more crystal oscillators (XOs) to generate these signals. An example is shown in Figure 1. Notice that generally an XO is needed for each clock signal. In contrast, Figure 2 shows synthesis of the same clock signals using just one Microsemi ZL30251.

The key disadvantages of the multiple-XO solution in Figure 1 include:

- Size. The XOs together are much larger than the 5x5mm ZL30251. This increases the size of the circuit board and increases total cost. Four 5x3.2mm XOs use *2.5* times the area used by ZL30251.
- Reliability. The failure rate of each XO is at least 30 times higher than the ZL30251.

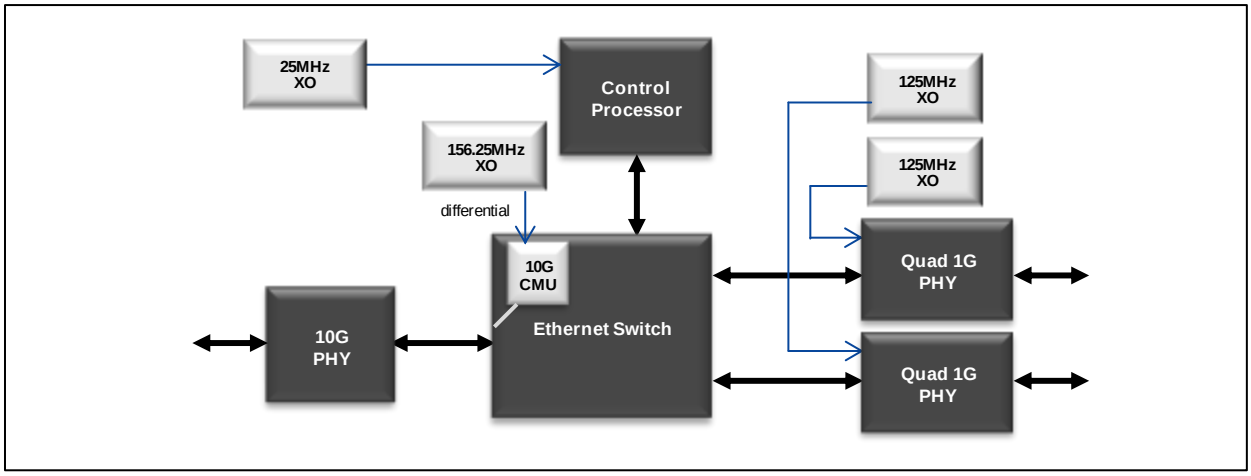


Figure 1 - Clock Synthesis for an Ethernet System Using XOs

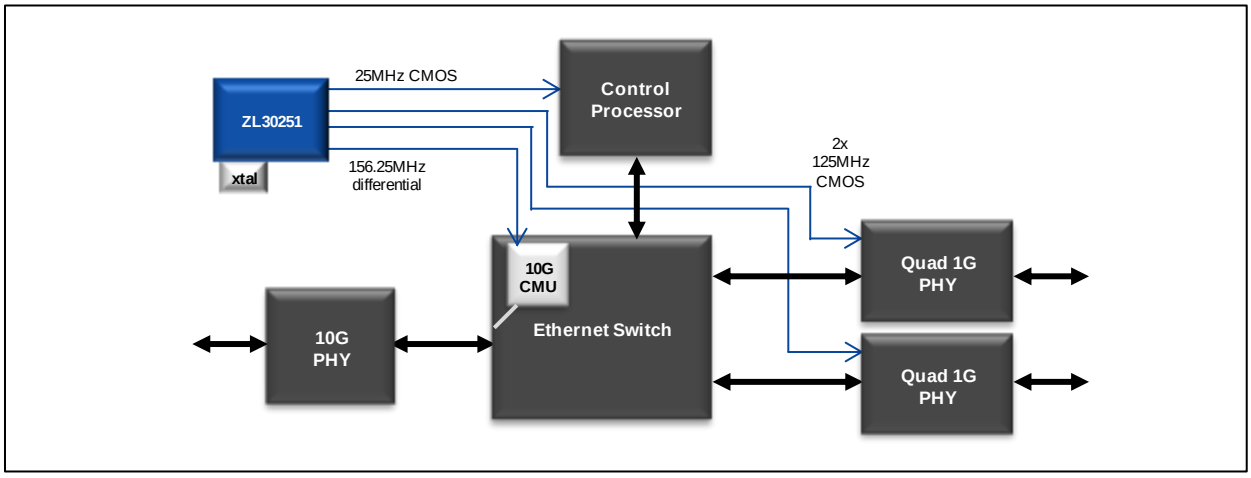


Figure 2 - Clock Synthesis for an Ethernet System Using Microsemi's ZL30251

The ZL30251 replaces multiple XOs with no disadvantage. With its ability to self-configure from internal nonvolatile memory, the ZL30251 can start generating its clock signals immediately after power-up, just like the XOs do. In addition, the ZL30251 can offer many other benefits:

ZL30251 Additional Benefits vs. Crystal Oscillators

Lower jitter than most XOs ○ Integer multiply as low as 0.16ps (12kHz-20MHz) ○ Fractional multiply typically less than 0.3ps (12kHz-20MHz)
Clock phase adjustment ○ Can be used to fix set-up and hold problems
Clock frequency adjustment ○ Any known error in the crystal frequency can be digitally compensated. ○ Frequency can be temporarily increased to perform frequency margining on data path components.
Glitchless start and stop of clock signals
One part number for many designs ○ Synthesizes any frequency from <1Hz to 1.035GHz with 0ppm error. ○ Creates the right clock signals using multi-format, multi-voltage output drivers. In contrast, any change in frequency, signal format, or voltage is a new part number for XOs.

Clock Multiplication and Frequency Conversion

Many electronic systems need clock signals that are frequency-locked to other clock signals rather than synthesized from a crystal. In some cases the output clock simply needs to be an integer multiple of the reference clock. An example of this from telecom transport systems is starting with a 19.44MHz reference clock and making 622.08MHz clock signals (multiply by 32). In other cases the system design requires multiplication of the reference clock frequency by a non-integer value. The ZL30251, discussed in the frequency synthesis section above, can also serve in a wide variety of clock multiplication and frequency conversion applications.

In Figure 3 the system designer had previously developed a board that includes Microsemi's ZL30153. The ZL30153 is familiar and is on the approved component list, and the designer wants to use it again for a new board design. For this new board, however, the clock requirements include three different frequency families, but the ZL30153 can only produce two. To solve this problem the designer has chosen to add a ZL30251 to make the third frequency family. In this application the designer can even decide to avoid the need for new board-level software to support the ZL30251 by asking Microsemi for a part number that ships pre-programmed for the application. This minimizes the engineering effort and gets the new board to market faster.

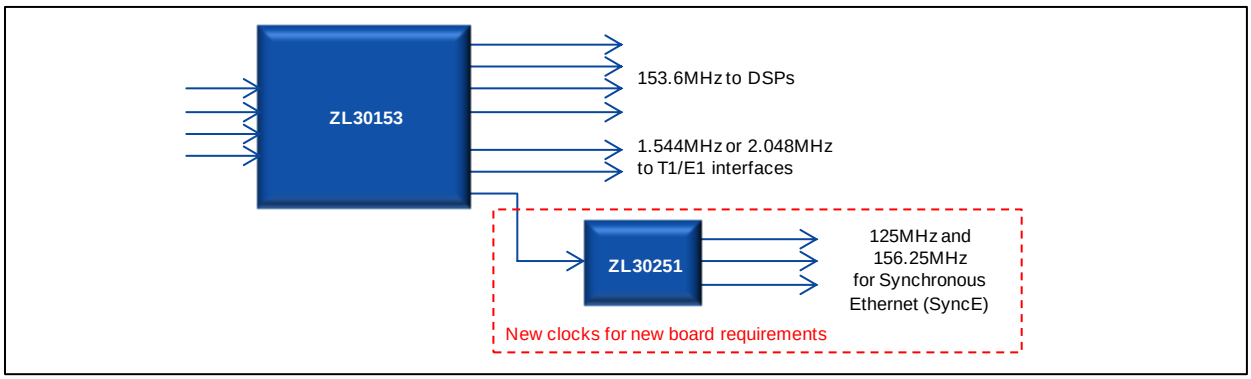


Figure 3 - Add-On Frequency Conversion Using Microsemi's ZL30251

The ZL30251 in Figure 3 is an APLL-only product. Like most APLL ICs, its minimum input frequency is about 10MHz. For applications that require frequency conversion from kHz reference clocks, the DPLL+APLL ZL30253 can be used instead. The ZL30253 has all the features of the ZL30251 and many more. An example application—a professional video camera—is shown in Figure 4 below. In this system the ZL30253's input clock is a horizontal sync signal. The ZL30253 multiplies this low-frequency input clock up to 74.25MHz and 148.5MHz or those frequencies divided by 1.001, depending on the broadcast video standard being used.

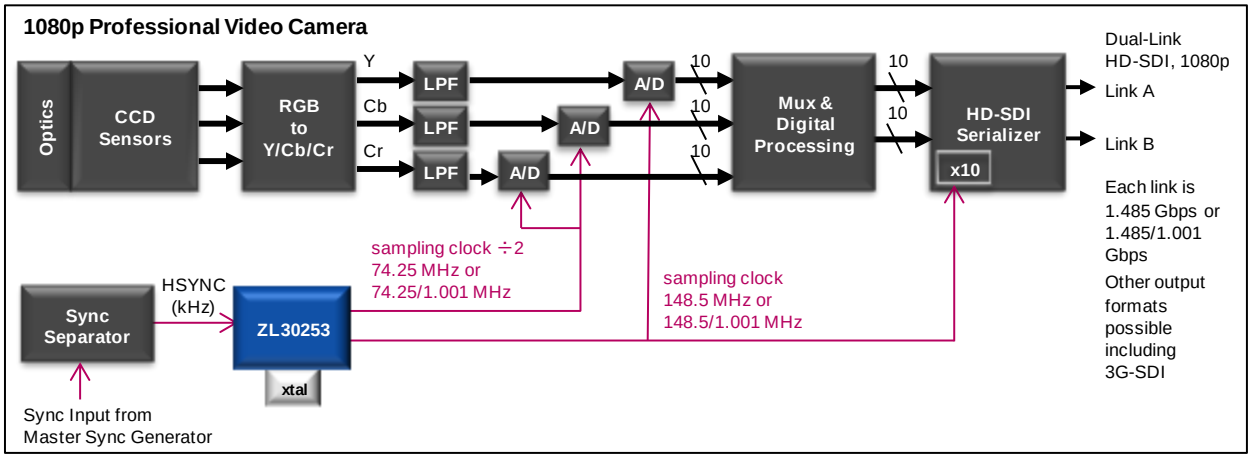


Figure 4 - Frequency Conversion from Low-Frequency Input Clock Using Microsemi's ZL30253

Frequency Conversion with Jitter Attenuation

As data rates continue to rise on a variety of system interfaces, the allowable jitter shrinks on interface reference clock signals. Leading-edge interface ICs now require reference clock jitter to be less than 0.3ps RMS, down from 1ps just a few years ago. This progression increases the need for jitter reduction (*attenuation*) at key points in system designs. For one example refer back to the professional video camera in Figure 4. The ZL30253's DPLL+APLL architecture enables it to perform both clock multiplication and jitter attenuation at the same time. This means that, regardless of the jitter of the HSYNC signal, the jitter of the output 74.25MHz and 148.5MHz signals is quite low. The ZL30253 does this by using a crystal and an internal crystal driver circuit as the *jitter* reference for the output clocks while the input reference clock signal is only used as the *frequency* reference for the output clocks.

For another example of jitter attenuation, see Figure 5, which is similar to Figure 3. In this case the designer has learned that the new family of clock signals must have lower jitter than can be provided by ZL30153+ZL30251. To address this he switches from the ZL30251 to the pin- and register-compatible ZL30253 plus a low-cost crystal.

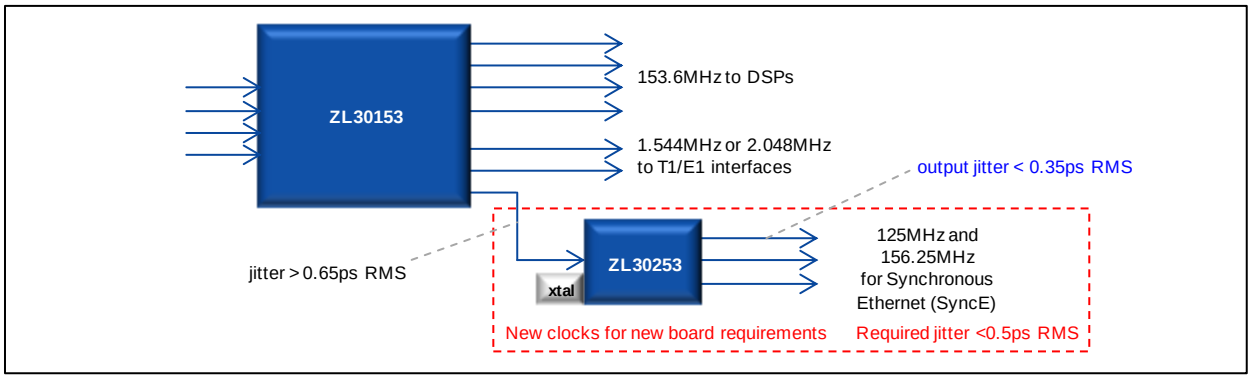


Figure 5 - Add-On Frequency Conversion and Jitter Attenuation Using Microsemi's ZL30253

Summary

Microsemi's family of 5x5mm clock synthesis, frequency conversion and jitter attenuation products show their versatility and performance in these applications and many more.

Key benefits include:

- Replacement of oscillators with smaller, higher-reliability ICs
- Any-to-any frequency conversion with output frequencies from 1Hz to 1GHz
- Jitter attenuation and industry-leading output jitter
- Easy to add to a board design when clock requirements expand
- Quick and easy change among product family members (all are pin- and register-set compatible)
- Ready to operate at system start (auto-configuration from nonvolatile memory)

Feature	ZL30250 / ZL30251	ZL30252 / ZL30253
Clock Synthesis	Y	Y
Any-to-Any Frequency Conversion, 0ppm error	Y	Y
Multi-Format, Multi-Voltage Clock I/O	Y	Y
Numerically Controlled Oscillator Mode	Y	Y
Jitter Attenuation		Y
Input Activity Monitoring		Y
Input Frequency Monitoring, %		Y
Internal Nonvolatile Memory	251 only	253 only
Number of Inputs	3 Universal Differential or Single-Ended	
Number of Outputs	Up to 3 Differential, Up to 6 CMOS	
Package	5x5mm QFN, Same Pinout for All Products	

Figure 6 – Product Family Comparison Table