Clock Translators for Optical Transport Networks

Optical Transport Network (OTN) has emerged as the physical layer interface protocol of choice, enabling carriers to bridge the transition from circuit-switched to internet protocol (IP), legacy transmission of voice over optical fiber or packet-switched transmission of data over optical fiber. Due to the variety of services and provisions, OTN timing solutions must be flexible and easily programmable to support multiple unique and independent channel frequencies.

Microsemi offers the widest portfolio of single-chip devices delivering "any rate, any port, all the time" performance for OTN.

For OTN equipment, Microsemi phase locked loops (PLLs) are used for line card timing including:

- Clock rate translation from line to client rates
- One PLL path per client port
- Clock rate programmability per client port

Features

Highly-integrated and programmable solution provides translation from any input reference frequency to any output clock frequency with jitter performance for interfaces 10G, 40G, and 100G coherent.

The single, dual, triple, and quad channel devices with independent digital PLLs accept and generate any frequency from 1 kHz to 1.25 GHz to support any communication service over optical networks.

OTN Requirements

- Multiple clock frequencies to support multiple services
- Dynamic rate conversion for forward error correction (FEC)
- Independent timing paths to support multiple transmit and receive services
- Stringent low jitter generation

Product Solutions

- Single-chip solutions compliant to the telecom timing standards
- Meeting OTN multi-service requirements
- Highly-integrated to support multiple OTN frequencies and channels
- Output jitter of 0.25 ps RMS

### Transponder and Muxponder Applications
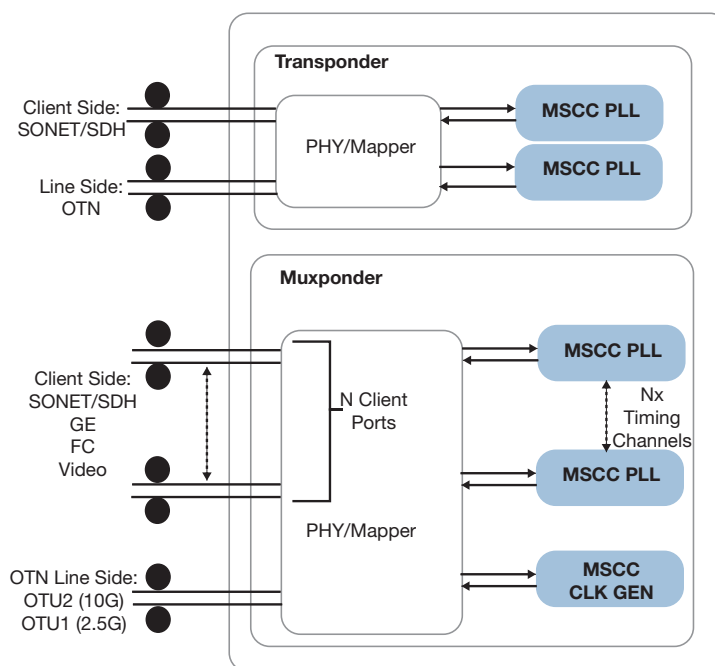
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Featured Products

ZL30169: 3-Input, 3-Output Clock Translator for OTN

- Any input frequency from 1 kHz to 1.25 GHz
- Continuous input clock quality monitoring
- Hitless reference switching on loss of input
- Programmable bandwidth: 14 Hz to 500 Hz
- Output jitter typically 0.16 ps RMS (APLL only. Output jitter for other modes: 0.25 ps RMS)
- Small package: 5 mm x 5 mm

ZL30169 Block Diagram
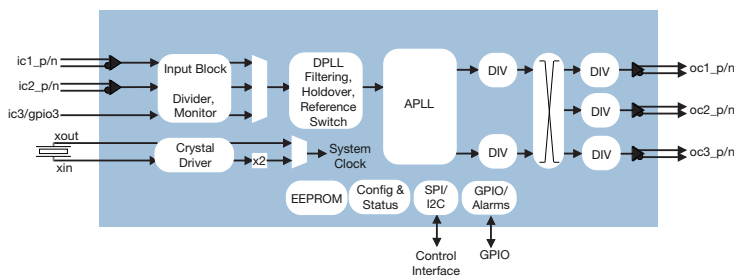
ZL30174: Triple Channel Precision Clock Translator

- 3 independent OTN de-synchronizers
- Excellent jitter performance of 180 fs RMS in 12 kHz to 20 MHz band meets jitter requirements of 10G/40G and 100G PHYs
- 3 programmable ultra-low jitter synthesizers generate any frequency from 1 Hz to 900 MHz
- 6 differential (CML) or 12 single-ended (CMOS) ultra-low jitter outputs, plus 2 general purpose CMOS outputs
- Accepts up to 10 LVPECL/LVDS/HCSL/LVCMOS inputs
- Automatic hitless reference switching and digital holdover on reference fail with initial holdover accuracy better than 10 ppb

ZL30174 Block Diagram
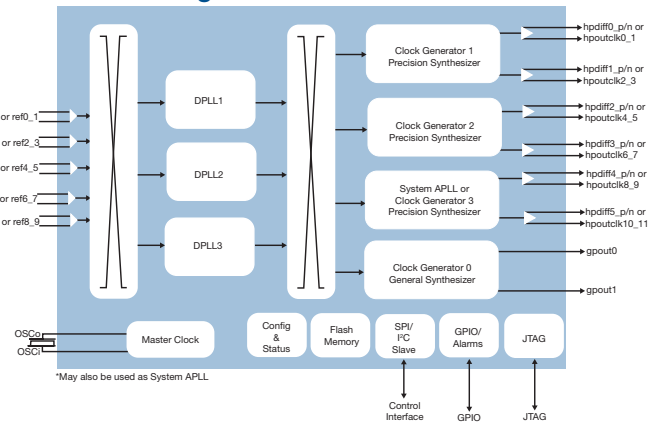
OTN Product Chart

	ZL30152	ZL30155	ZL30157	ZL30160	MAX24705 MAX24710	ZL30169	ZL30182	ZL30174	ZL30614
PLL Channels	1	2	2	4	1	1	2	3	4
Synthesizers	1 precision	2 precision	1 precision 1 general	2 precision 2 general	2 precision	1 precision	2 precision	3 precision 1 general	3 precision 1 general
Any Clock Rate	1 KHz– 750 MHz	1 KHz– 750 MHz	1 KHz– 750 MHz	1 KHz– 750 MHz	1 KHz– 750 MHz	1 Hz– 1035 MHz	1 Hz– 1035 MHz	1 Hz– 900 MHz	0.5 Hz– 900 MHz
Jitter	700 fs	700 fs	700 fs	700 fs	350 fs	250 fs	250 fs	180 fs	180 fs

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