Crystal Circuit Design Guide for MAX24000 Series, ZL30151, ZL30169, ZL30182, ZL30244, ZL30245, ZL3025x, ZL30621, and ZL40255 Series

Introduction

This document details how to select the components for the external crystal oscillator circuit used by the MAX24000 Series, ZL30151, ZL30169, ZL30182, ZL30244, ZL30245, ZL3025x, ZL30621, and ZL40255 Series of any-to-any clock multipliers, jitter attenuators, and telecom timing integrated circuits (ICs).

Component Selection

Figure 1 shows the external crystal oscillator circuit for the ZL30151, ZL30169, ZL30182, ZL30244, ZL30245, ZL3025x, ZL30621, and ZL40255 Series of devices. Figure 2 shows the external crystal oscillator circuit for the MAX24000 Series of devices. The circuits are identical except for the IC pin names. The same component selection process is used for both circuits.

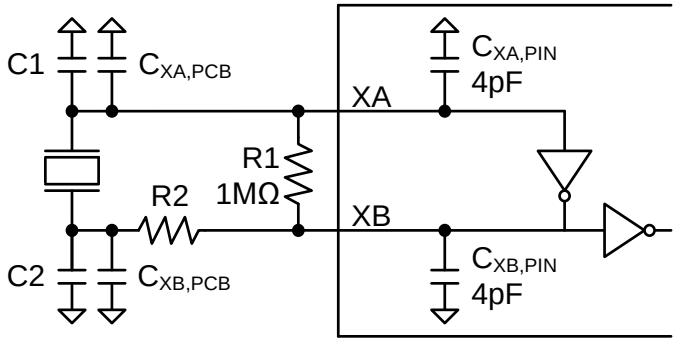

Figure 1 ZL30151, ZL30169, ZL30182, ZL30244, ZL30245, ZL3025x, ZL30621, ZL40255 Series External Crystal Oscillator Circuit

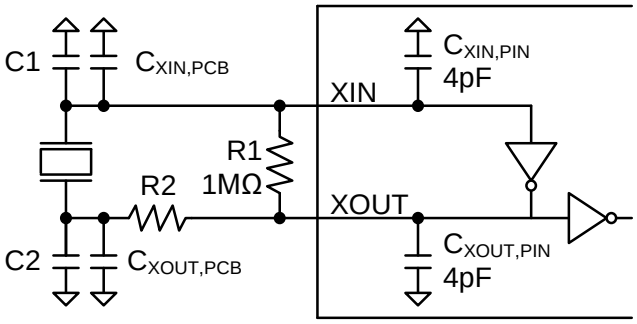

Figure 2 MAX24000 Series External Crystal Oscillator Circuit

The crystal should be a fundamental mode, AT-cut crystal resonator that meets the specifications listed in Table 1 · . Additionally, the following guidelines for crystal frequency selection should be used to achieve the best possible output clock jitter performance:

- For APLL-only operation, integer multiplication (APLL input frequency * N = APLL VCO frequency) gives lower output clock jitter than fractional multiplication. Choose a crystal frequency that allows the APLL to do integer multiplication to achieve the best output clock jitter performance.
- All else being equal, a higher APLL input frequency yields lower output clock jitter. Choose the highest possible crystal frequency to achieve the best output clock jitter performance. This guideline is secondary to choosing a frequency that allows integer multiplication.
- When using the APLL to perform fractional multiplication, choose a crystal frequency of at least 49 MHz to achieve the best output clock jitter performance.

Table 1 · Crystal Selection Parameters

Parameter		Symbol	Min.	Typ.	Max.	Units
MAX24000 Series Crystal Oscillation Frequency[1]		f_{osc}	25	–	52	MHz
ZL30151, ZL30169, ZL30182, ZL30244, ZL30245, ZL3025x, ZL30621, ZL40255 Series Crystal Oscillation Frequency[1]		f_{osc}	25	–	60	MHz
Shunt Capacitance		C_O	–	2	5	pF
Load Capacitance		C_L	–	10		pF
Equivalent Series Resistance (ESR)[2]	f_{osc} < 40 MHz	R_S	–	–	60	Ω
	f_{osc} > 40 MHz	R_S	–	–	50	Ω
Maximum Crystal Drive Level			100	–	–	µW

Notes:

1. *Higher frequencies give lower output jitter, all else being equal.*
2. *These ESR limits are chosen to constrain crystal drive level to less than 100µW. If the crystal can tolerate a drive level greater than 100µW then proportionally higher ESR is acceptable.*

The value of resistor R1 is fixed at 1 MΩ. The value of resistor R2 is a function of both the crystal frequency and power rating. Table 2 · specifies how to choose R2 for a given crystal. The lowest valid R2 resistance in Table 2 · should be chosen to achieve the best output clock jitter performance.

The value of capacitors C1 and C2 are chosen to achieve a crystal load capacitance (C_L) of 10pF. C1 is chosen such that the total capacitance on pin XA/XIN is 20pF. Capacitance sources include the device's internal pin capacitance of 4pF, the associated printed circuit board (PCB) trace capacitance, and capacitor C1. The following formula can be used to calculate the value of C1:

$$C1 = 20pF - C_{XA,PCB} - C_{XA,PIN=4pF}$$

Similarly, C2 is chosen such that the total capacitance on pin XB/XOUT is 20pF. Unlike the XA/XIN pin, the effective capacitance of pin XB/XOUT is a function of the crystal frequency, crystal power rating, and impedance of R2. Table 2 · specifies how to determine the effective XB/XOUT pin capacitance, $C_{XB,PIN}$, for a given crystal. The following formula can be used to calculate the value of C2:

$$C2 = 20pF - C_{XB,PCB} - C_{XB,PIN} \text{ (where, } C_{XB,PIN} \text{ comes from Table 2 ·)}$$

Table 2 · R2 and Effective XB/XOUT Pin Capacitance vs. Crystal Frequency and Power Rating

Freq (MHz)	$C_{XB,PIN}$, Effective XB/XOUT Pin Capacitance (pF)							
	Crystal = 300 µW		Crystal = 200 µW		Crystal = 100 µW			
	R2=300 Ω	R2=400 Ω	R2=700 Ω	R2=750 Ω	R2=1.3k Ω	R2=1.5k Ω	R2=1.6k Ω	R2=1.7k Ω
25	3.3	3.3	-	3.2	-	-	-	2.7
30	3.3	3.3	-	3.1	-	-	-	2.5
35	--	3.2	-	3.0	-	-	-	2.3
40	--	3.2	2.9	2.9	-	-	2.2	2.1
45	--	3.1	2.8	2.8	-	2.1	2.0	2.0
50	--	3.0	2.7	2.7	-	2.0	1.9	1.8
55	--	3.0	2.6	2.6	2.0	1.9	1.8	1.7
60	--	2.9	2.5	2.5	1.9	1.8	1.7	1.6

Note: A table entry of "--"corresponds to an invalid operating point where the maximum power dissipation of the crystal is exceeded.

Crystal Circuit Design Example

As an example of how to select the external crystal oscillator circuit component values, consider the case of using a ZL30251 to synthesize output clock frequencies of 156.25 MHz, 125 MHz, and 25 MHz from a crystal reference. In order to achieve the lowest output clock jitter, APLL integer multiplication mode is used. In this mode, two crystal frequency options that could be used to achieve the specified list of output clock frequencies are 25 MHz and 50 MHz. Of these options, the higher-frequency 50 MHz crystal is chosen to achieve the best output clock jitter performance. Assuming a crystal power rating of 100 µW and 1.5pF of PCB trace capacitance on both XA/XIN and XB/XOUT, the circuit resistor and capacitor values are:

R1 = 1 MΩ (fixed)

R2 = 1.5 kΩ (lowest R2 value is in the 100 µW headings of Table 2 · for 50 MHz crystal)

$C_{XA,PIN}$ = 4pF (fixed)

$C_{XB,PIN}$ = 2pF (from Table 2 · , 100 µW section, 50 MHz row, R2=1.5 kΩ column)

$C_{XA,PCB}$ = 1.5pF

$C_{XB,PCB}$ = 1.5pF

C1 = 20pF – 1.5pF – 4pF = 14.5pF

C2 = 20pF – 1.5pF – 2pF = 16.5p

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