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# Recommended Power Supply Decoupling and Layout Practices for the MAX24000 Series

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## Introduction

This document details the recommended power supply decoupling and layout practices for the MAX24000-series any-to-any clock multipliers, jitter attenuators and telecom timing IC's. This series of devices includes the MAX24205, MAX24210, MAX24305, MAX24310, MAX24405, MAX24410, MAX24505, MAX24510, MAX24605, MAX24610, MAX24705, and MAX24710.

## Power Supply Decoupling and Layout Practices

The following common design practices are recommended for improving device power supply noise rejection.

- Use power islands to isolate and filter analog power supply connections. MAX24xxx output clock jitter may increase if the device is exposed to excessive noise on its analog power pins. For optimal jitter performance, these pins should be isolated from their respective board supplies using power islands. A power island is a local copper area which is separated from the main power plane by a series passive component. Its purpose is to provide improved isolation from noise on the board power planes. Each MAX24xxx power island should be tied to its respective board power plane at a single point through a ferrite bead. The ferrite bead provides suppression of digital switching noise generated by other integrated circuits connected to that power plane. The ferrite bead should have a resistance of several hundred ohms at 100 MHz. Additionally, it should have a current rating at least double the maximum current required by the island to avoid core saturation and degraded performance. Ferrite beads have a small DC resistance which will cause the island supply voltage to be lower than the main power plane voltage. This voltage drop must be taken into account when designing the device power supplies. The Murata BLM18PG471SN1 is one example of a ferrite bead which can be used for this purpose.
- Allocate one low ESR 0.1 $\mu$ F decoupling capacitor for each power pin. Example recommended capacitor types are ceramic X5R and X7R. Each capacitor should be located as close as possible to its respective device power pin. Each capacitor should only be connected directly to that power pin and should not share vias to power or ground planes with other decoupling capacitors.
- Allocate two low ESR bulk capacitors, 1 $\mu$ F and 10 $\mu$ F, for each device power domain. The power domains consist of each device analog power island and the device's 1.8 V and 3.3 V digital supplies. Example recommended capacitor types are ceramic X5R and X7R. Tantalum capacitors can also be used. These capacitors filter low frequency noise (up to several hundred kHz) that originates from switching power supplies. For the analog power islands, these capacitors should be located close to the ferrite bead which ties the power island to its respective power plane. For the digital supplies, these capacitors should be located close to the device and can be shared with nearby devices to reduce component count.

- When using an external crystal resonator connected to the device's XIN and XOUT pins, the crystal driver power pins VDD\_XO\_18 and VDD\_XO\_33 should each have a dedicated power island to achieve the best jitter performance. In addition to the capacitors listed above, allocate a low ESR 100 $\mu$ F capacitor for each of these power islands. Example recommended capacitor types are ceramic X5R and X7R. Tantalum capacitors can also be used. This capacitor should be located close to the ferrite bead which ties the power island to its respective power plane. If an external crystal reference is not used, the crystal driver power pins can be tied to the corresponding device core supply voltage power islands.
- Connect all device ground pins to a common ground plane.

The MAX24xxx has four output clock banks, A through D, which are independently powered for output signal format flexibility. The corresponding device power pins are VDDOA, VDDOB, VDDOC, and VDDOD. When implementing the above guidelines, any output clock bank requiring a 3.3 V or 1.8 V supply can share a power island with the corresponding device core analog supply voltage. If an output clock bank requires a supply voltage other than 1.8 V or 3.3 V, an additional power island and associated filtering circuitry is required for that bank. This power island can be shared with other output clock banks requiring the same supply voltage.

[Figure 1 on page 3](#) illustrates the application of these guidelines to a design which uses an external XO and has all device output clock banks powered by 3.3 V. [Figure 2 on page 4](#) illustrates the application of these guidelines to a design which uses an external crystal resonator and has all device output clock banks powered by 3.3 V.

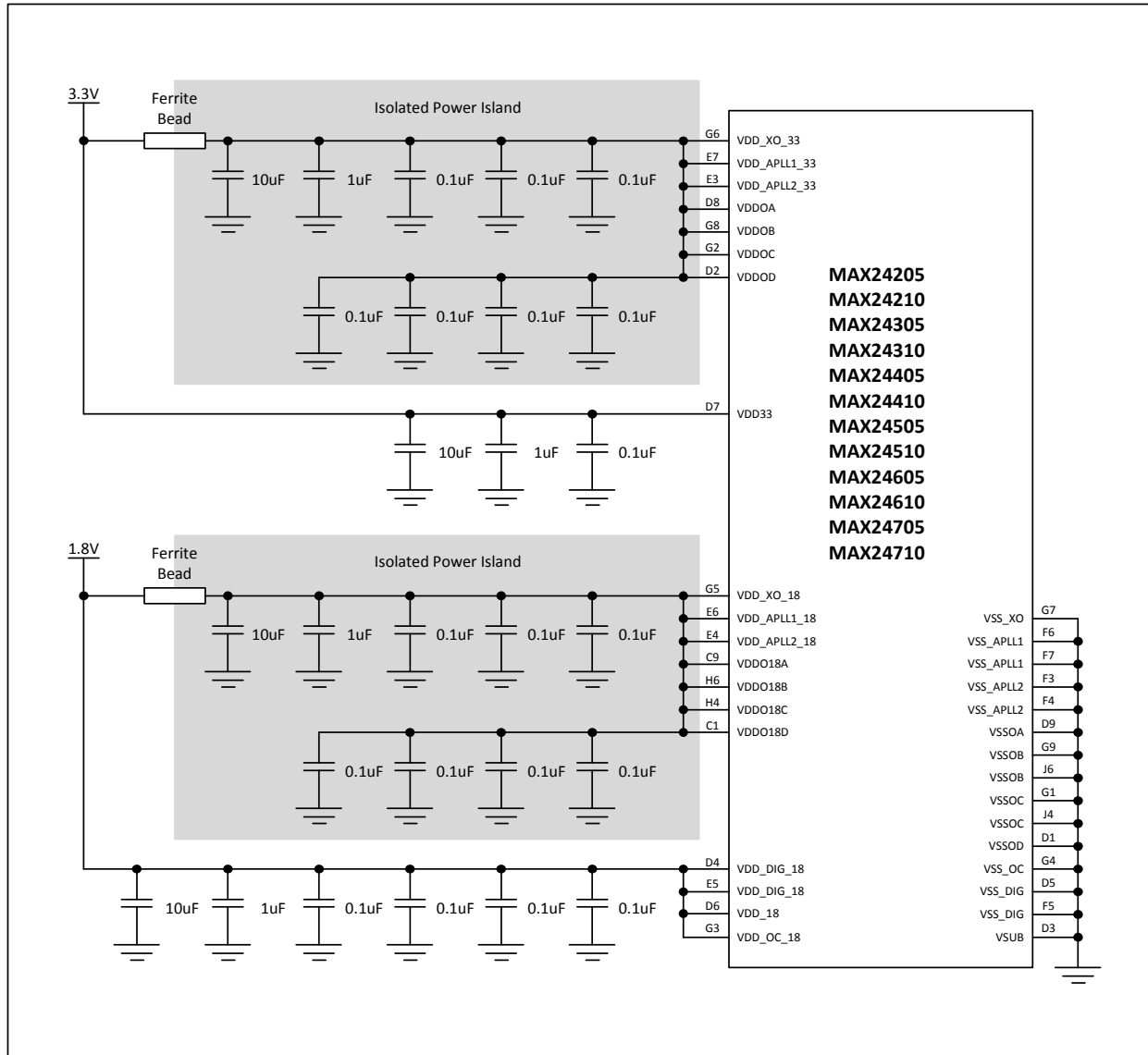


Figure 1 Example MAX24xxx Power Supply Decoupling When Using an External XO

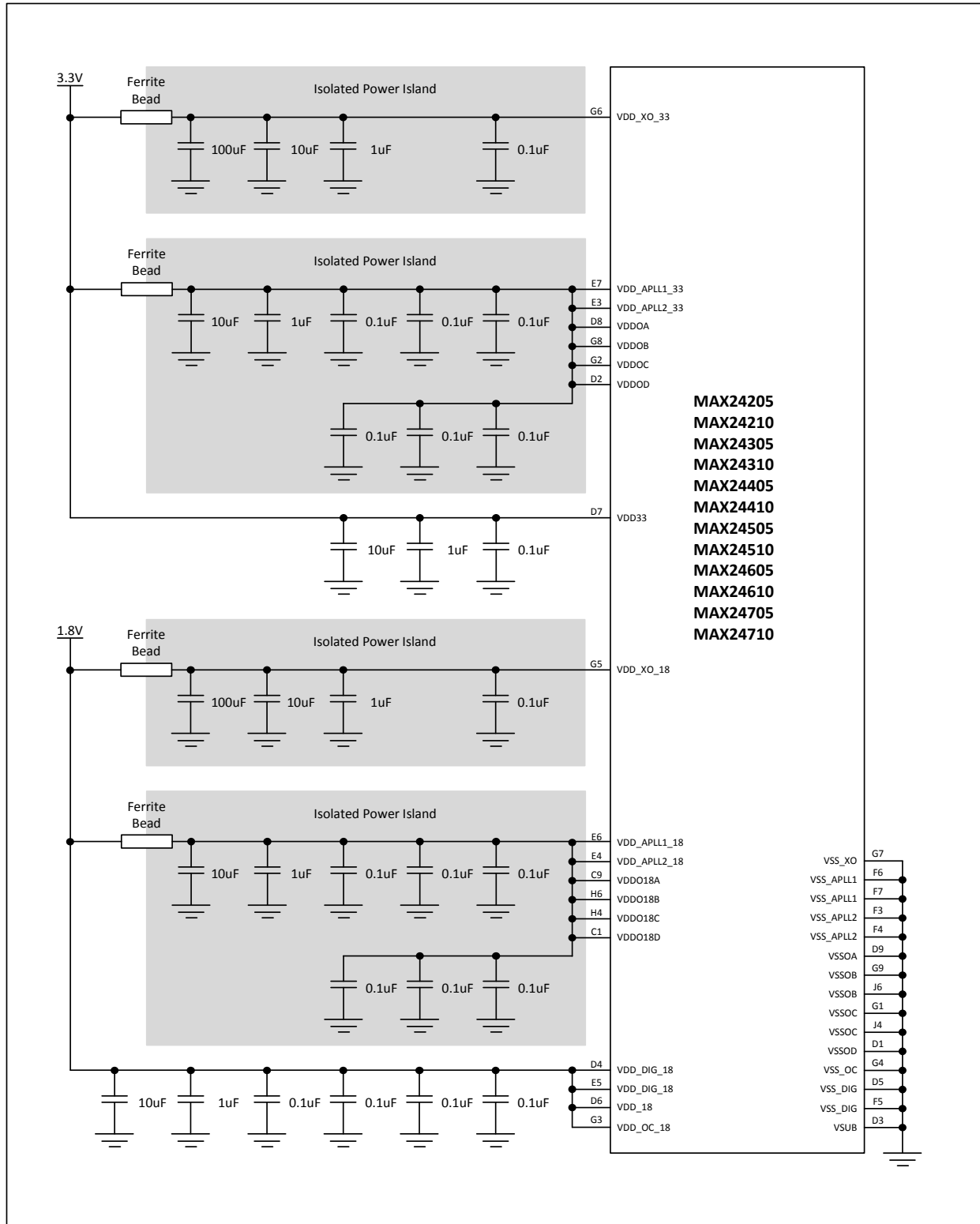
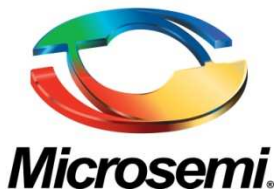


Figure 2 Example MAX24xxx Power Supply Decoupling When Using an External Crystal Resonator



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