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# Electro-Static Discharge

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## Introduction

All electronic integrated circuit (IC) devices are susceptible to damage from static electricity or electrostatic discharge (ESD). While some devices can withstand thousands of volts of ESD before damage, others may have a threshold of only a few volts.

There are three primary models in the industry used today to describe the charge transfer during an ESD event: Human Body Model, Machine Model, and Field-Induced Charged Device Model.

## Human Body Model (HBM)

The Human Body Model is the oldest and most commonly used model for classifying device sensitivity to ESD. It was devised to simulate the effect of an ESD event from the finger of a charged, human body contacting a component lead. This model and the available test methods are described by the following standards and revisions:

- MIL-STD-883: TM3015.7
- JEDEC: JESD22-A114C.01
- ESD Association: STM5.1
- Automotive Electronics Council: AEC - Q100-002

Actel utilizes the MIL-STD-883 test method for 883 qualified devices and the JEDEC test method for commercial and industrial grade devices.

## Machine Model (MM)

The human body is not the only source capable of being triboelectrically charged. In the machine model, the charge source is assumed to be a piece of equipment or a tool that has become charged through use, which then comes into contact with a component lead. The MM was developed to describe ESD events that can occur during the manufacturing process. This model and the test methods are described by the following standards and revisions at the time of writing:

- JEDEC: JESD22-A115-A
- ESD Association: STM5.2

When MM testing is done for Actel devices, the JEDEC test method is used.

## Field-Induced Charged Device Model (CDM)

The third major ESD transfer model is the charged device model. The goal of CDM testing is to simulate the discharge from the device through mechanical means when it contacts a low impedance ground or charge sink. Such a discharge can occur when a device slides down a feeder tube during board assembly. This model and the test methods are described by the following standards and revisions at the time of this writing:

- JEDEC: JESD22-C101C
- ESD Association: STM5.3.1

When CDM testing is done for Actel devices, the JEDEC test method is used.

## ESD Sensitivity Classification

Based upon the test results, a device can be categorized by ESD sensitivity. Table 1 gives the classification level for the HBM under the JEDEC specification. Table 2 gives the classification level for the HBM under the MIL-STD-883 specification.

Table 1 • JEDEC: JESD22-A114C.01 ESD Sensitivity Classification

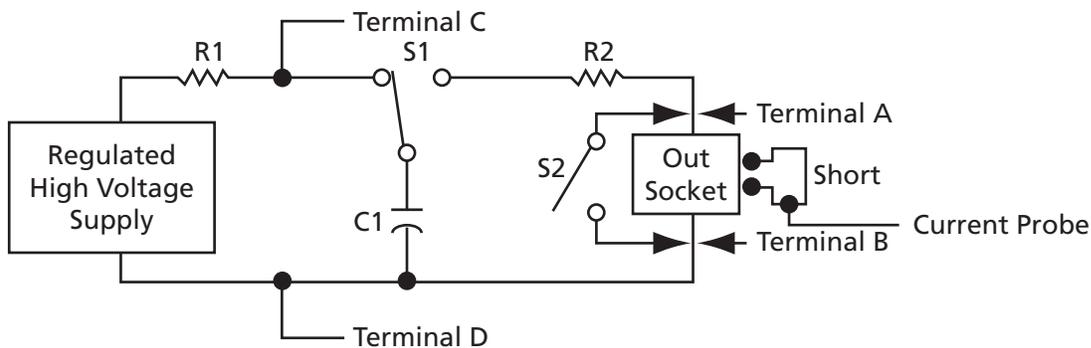
Classification	Successful Device ESD Performance
Class 0	Less than 250 V
Class 1A	250 V to 500 V
Class 1B	500 V to 1000 V
Class 1C	1000 V to 2000 V
Class 2	2000 V to 4000 V
Class 3A	4000 V to 8000 V
Class 3B	Greater than 8000 V

Table 2 • Mil-883 ESD Sensitivity Classification

Classification	Successful Device ESD Performance
Class 1	0 V to 1999 V
Class 2	2000 V to 3999 V
Class 3	4000 V and above

## ESD Test Method

ESD testing of the eX/SX-A/RTSX-S/RTSX-SU devices has been performed in compliance with the requirement of the MIL-STD-883 test method 3015.7. The test setup is described in Figure 1.



- R1 =  $10^6 \Omega$  to  $10^7 \Omega$
- C1 = 100 picofarads  $\pm 10\%$  (Insulation resistance  $10^{12} \Omega$  minimum)
- R2 =  $1,500 \Omega \pm 1\%$
- S1 = High voltage relay (Bounceless, mercury-wetted, or equivalent)
- S2 = Normally closed switch (Open during discharge pulse and capacitance measurement)

Figure 1 • MIL-STD-883 TM3015.7 Test Setup

## Pin Grouping During ESD Testing

During ESD Test Method 3015.7 testing, the various pins on the device are grouped together based on their functionality. The groupings are as follows:

- All I/Os (including JTAG) grouped = I/O
- All ( $V_{CCA}$ ,  $+V_{PP}$  +  $V_{SV}$ <sup>1</sup>) grouped = Power Group  $V_{CCA}$
- All  $V_{CCI}$  grouped = Power Group  $V_{CCI}$
- All GNDs ( $GNDQ$ ,  $GNDI$ ,  $GND A$ , and  $V_{KS}$ <sup>2</sup>) grouped = Power Group GND

## Test Method 3015.7 Sequence

1. Program devices with Qualification Burn-In (QBI) design.
2. Prestress functional ATE test at Actel
3. Prestress curve trace (at vendor site)
  - If the pin is an I/O, sweep  $-1.5$  V to  $+1.5$  V with respect to GND, limiting current to  $50$   $\mu$ A.
  - If the pin is an I/O, sweep  $-1.5$  V to  $+1.5$  V with respect to  $V_{CCI}$ , limiting current to  $50$   $\mu$ A.
  - If the pin is an I/O, sweep  $-1.5$  V to  $+1.5$  V with respect to  $V_{CCA}$ , limiting current to  $50$   $\mu$ A.
  - If the pin is  $V_{CCI}$ , sweep  $-1.5$  V to  $+1.5$  V with respect to GND, limiting current to  $50$   $\mu$ A.
  - If the pin is  $V_{CCA}$ , sweep  $-1.5$  V to  $+1.5$  V with respect to GND, limiting current to  $50$   $\mu$ A.
  - If the pin is  $GND A$ ,  $GND I$ , or  $GND Q$ , sweep  $-1.5$  V to  $+1.5$  V with respect to  $V_{CCA}$ .
  - If the pin is  $GND A$ ,  $GND I$ , or  $GND Q$ , sweep  $-1.5$  V to  $+1.5$  V with respect to  $V_{CCI}$ .
  - The failure criteria is 15% shift in current.
- Zap sequence
  - Individual pins of the I/O,  $V_{CCI}$ , and  $V_{CCA}$  (Zap Terminal) vs. GND (Ground Terminal)
  - Individual pins of the I/O, GND, and  $V_{CCA}$  (Zap Terminal) vs.  $V_{CCI}$  (Ground Terminal)
  - Individual pins of the I/O, GND, and  $V_{CCI}$  (Zap Terminal) vs.  $V_{CCA}$  (Ground Terminal)
  - Individual pins of the I/O (Zap Terminal) vs. I/O (remaining pins in group) (Ground Terminal)
- Order
  - Numerical starting at Pin 1.
  - Three positive pulses are applied.
  - Curve trace is then performed.
  - If the pin passes the curve trace, then three negative pulses are applied, followed by another curve trace.
    - If the pin fails the curve trace, the pin is pulled and not zapped anymore.
    - Fresh device is started at the next lower zap voltage.
    - The requirement is for each of the three devices to pass every combination (no substitutions allowed).
- Back to Actel for post ATE test.

## eX, SX-A, RTSX-S, and RTSX-SU ESD Test Results

Using the test method described above, the eX devices were able to pass MIL-STD-883 TM3015.7 HBM ESD testing at 50 V. The SX-A, RTSX-S, and RTSX-SU devices were able to pass at 75 V.

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1.  $V_{SV}$  is connected to  $V_{CCA}$  during normal operation. In the datasheet, the  $V_{SV}$  pin will appear as a  $V_{CCA}$  pin.  
 2.  $V_{KS}$  is connected to GND during normal operation. In the data sheet, the  $V_{KS}$  pin will appear as a GND pin.

## Description of RTSX-S ESD Failure Mechanisms

During ESD testing, Actel has found that when the GNDQ and  $V_{K5}$  pin are included in the Power Group GND, the ESD damage occurs at test levels above 75 V. Actel has also determined that with the Power Ground GND, ESD damage occurs at test level above 75 V for the GNDQ pins and 250V for the  $V_{K5}$  pin. When the GNDQ and  $V_{K5}$  pins are excluded from the test groups, the ESD rating of the devices passes 2000 V. ESD levels described in the "eX, SX-A, RTSX-S, and RTSX-SU ESD Test Results" section on page 3 are observed only when a GNDQ pin is connected to the positive terminal of the tester, and the  $V_{CCI}$  pin group is connected to the negative terminal of the tester. No ESD failures have been observed at levels below 75 V.

There are two failure mechanisms associated with ESD, which were observed during testing. The first failure mechanism is an input stuck-at-one fault, where the output from the input pin buffer appears to be permanently high. The second failure mechanism is a shift in the  $V_{IH}$  threshold of an input cell. In both cases, analysis of damaged FPGAs has shown that damage has occurred in a specific transistor, known as the N3b transistor, in an I/O cell. The N3b transistor in each I/O cell is located between the GNDQ and  $V_{CCI}$  supplies. Refer to the schematic in Figure 2.

CDM testing per the JEDEC test method has identified failures in the same N3b transistor at levels above 250 V. JEDEC CDM testing at 250 V passed on all pins.

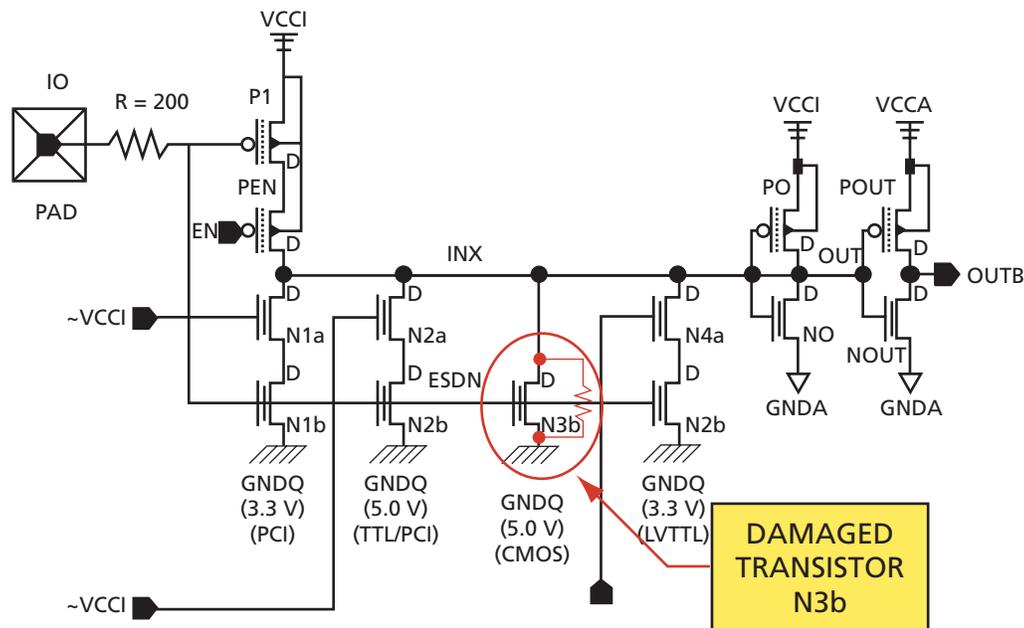


Figure 2 • User I/O Circuit Schematic

In the case of stuck-at-one faults, the N3b transistor exhibits a low-impedance path from source to drain, effectively shorting the transistor out and holding the output of the input buffer high. Figure 3 shows a Scanning Electron Microscopy (SEM) photograph of the damaged N3b transistor in a device that exhibited a stuck-at-one fault as a result of ESD damage.

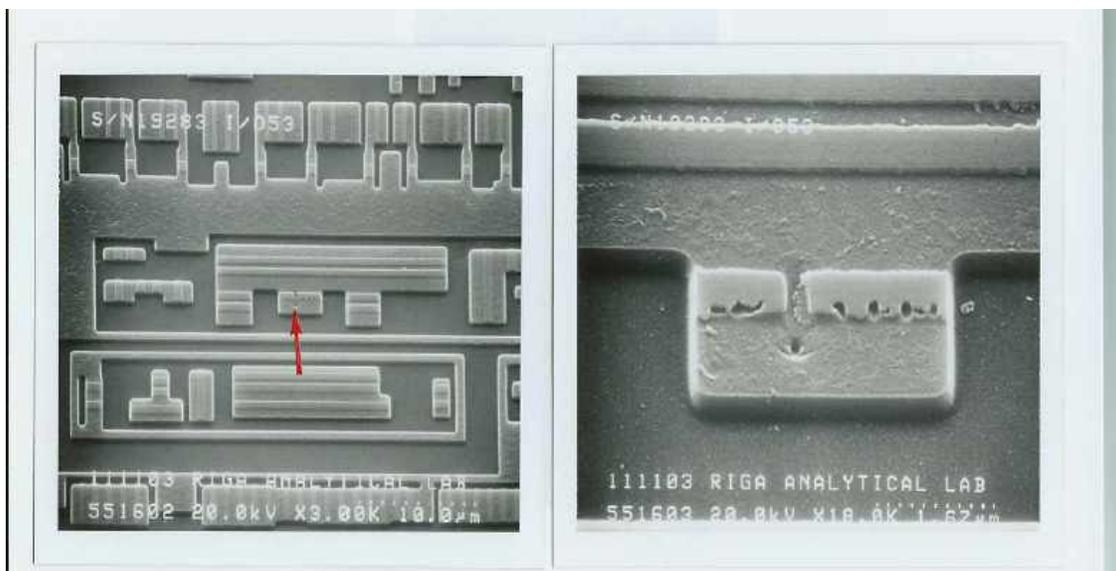


Figure 3 • SEM Photograph of Damaged N3b Transistor

In the case of a  $V_{IH}$  threshold shift, damage to the gate of the N3b transistor is observed, but is lesser in degree than damage that observed in the device exhibiting a stuck-at-one fault. The transistor characteristics are altered by the damage, but the transistor is still functional. Figure 4 shows a SEM photograph of the damaged N3b transistor in a device that exhibited a  $V_{IH}$  threshold shift as a result of ESD.

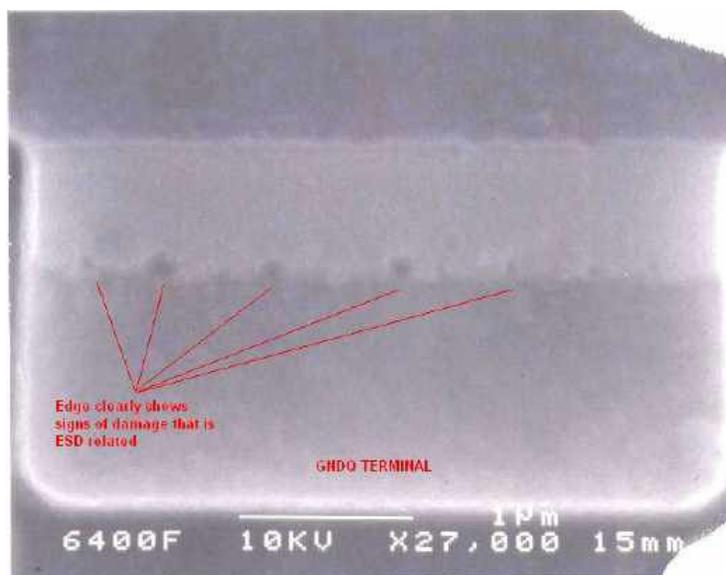


Figure 4 • SEM Photograph of Subtle Damage to N3b Transistor

Table 3 • Location of GNDQ Pins

Package Type	Pin Count	RT54SX325/RTSX325U	RT54SX725/RTSX725U	eX64	eX128	eX256	A54SX08A	A54SX16A	A54SX32A	A54SX72A
CQFP	208	1, 52, 105, 157	1,52,105, 157						1, 52, 105,157	1, 52, 105,157
	256	1, 59, 128, 189	1,59,128, 189						1, 59, 128,189	1, 59, 128, 189
CCLG	256 (finger)	2, 65, 138, 193								
	256 (LGA)	A15, C3, P2, R16								
CCGA	624		AA5, AA21, B3, D23							AA5, AA21, B3, D23
TQFP	64			1, 33	1, 33					
	100			1, 51	1, 51	1, 51	1, 51	1, 51	1, 51	
	144						1, 36, 73, 109	1, 36, 73, 109	1, 36, 73, 109	
	176									
PQFP	208					1, 52, 105, 157	1, 52, 105, 157	1, 52, 105,157	1, 52, 105, 157	
CS	49			C4, D3, D4, E4*	C4, D3, D4, E4*					
	128			B11, M1	B11, M2	B11, M1				
	180					A3, N2, P12, C12				
FBGA	144						B2, L1, K10, B11	B2, L1, K10, B11	B2, L1, K10, B11	
	256							C3, P2, R16, A15	C3, P2, R16, A15	C3, P2, R16, A15
	484							E5, AD3, AB21, D22	E5, AD3, AB21, D22	
PBGA	329							A2, C22, Y4, Y20		
PLL	84							2, 27, 42, 61*		

Note: \*GNDQ shorted to GND net.

## Probability of ESD Damage

There are only four GNDQ pads on each device. The probability of an ESD event causing damage to a device is dependent not only on the amplitude of the ESD event, but also on the probability of the ESD event when the GNDQ pin receives a positive charge with respect to a V<sub>CC1</sub> pin. This probability can be estimated by EQ 1.

$$\frac{\text{Number of GNDQ Pins}}{\text{Total Number of Pins}} \times \frac{\text{Number of V}_{\text{CC1}} \text{ Pins}}{\text{Total Number of Pins}}$$

EQ 1

For example, a 208-CQFP package has four GNDQ pins, eight V<sub>CC1</sub> pins, and 208 pins in total. Using the formula given above, the probability of an ESD event is shown in EQ 2.

$$\frac{4}{208} \times \frac{8}{208} = 0.074\%$$

EQ 2

## Device Handling Procedure

When handling the devices, care must be taken to ensure that the devices are not damaged by an ESD event. Actel recommends the following:

- "Electrostatic Protected Area (EPA)"
- "Personal Grounding"
- "ESD Protective Clothing/Smocks"
- "Air Ionizer"
- "Antistatic Solution"
- "Antistatic Floor Mats"
- "Identification"

### Electrostatic Protected Area (EPA)

A place designed to handle the ultra-sensitive ESD parts. This area is configured and maintained using the guidelines provided in ANSI/ESD S20.20. The guidelines recommend the following conditions are met and only trained personnel are allowed in the EPA:

- Floors with surface resistivities in the range of 10E4 to 10E6
- All the necessary equipment properly grounded
- Air ionizers
- Antistatic work surfaces with proper equipment (wrist straps, smocks, shoe straps, and gloves)

### Personal Grounding

A wrist strap or ESD cuff that is in constant contact with bare skin and has a cable for attaching it to the ESD ground must be worn at all times. In addition to a wrist strap, heel straps or ESD shoes must also be worn. The purpose of the wrist strap and heel straps is to drain off the operator's static charge.

### ESD Protective Clothing/Smocks

Even with the wrist strap, street clothing must not come in close contact with the devices. The various materials in clothing can generate high static charges. Because clothing is usually electrically insulated or isolated from the body, charges on clothing fabrics are not necessarily dissipated to the skin and then to ground. The ESD protective smock will serve as a barrier/shield to protect the devices. The ESD protective

smock must be buttoned whenever the user is at an ESD-protected workstation or in a designed ESD-protected area. The smock manufacturer's cleaning instructions must be followed to gain maximum effectiveness and utility from the smocks.

## Air Ionizer

An air ionizer must be used to neutralize static charges that can build up on insulated and isolated objects (objects that cannot be grounded). The air ionizer charges the molecules of the gases of the surrounding air. Any static charge that is present on the objects will be neutralized by attracting the opposite polarity charges from the air. Because it uses only the air that is already present in the work environment, an air ionizer may be employed even in clean rooms where chemical sprays and some static dissipative materials are not usable.

Air ionizers, when used, must conform to the following:

- Table ionizers must be positioned so that the devices at the ESD-protected workstations are within the ionizer manufacturer's specified coverage area. The ionizer must be aimed at the devices and operator's hands rather than at the operator.
- Ceiling ionizers must be oriented in relation to the work surfaces, in accordance with the ionizer manufacturer's instructions.
- Devices must not be brought closer to the ionizer than specified by the ionizer manufacturer.
- There must be an unrestricted, straight-line airflow between the ionizers and the unprotected devices.
- The ionizer balance (positive and negative ions) must be verified per ANSI standard EOS/ESD-S3.1.
- The ionizer charge decay performance must be verified using the method described in ANSI standard EOS/ESD-S3.1.

## Antistatic Solution

Antistatic chemicals (antistatic solutions) can be used to prevent static charge generation on static generating/charging materials in the work or storage areas. During application of any antistatic chemical, Actel recommends the following:

1. The antistatic solutions must be chosen to avoid contamination of ESD devices.
2. Antistatic spray or solutions must not be applied in any form to energized electrical parts, assemblies, panels, or equipment.
3. Antistatic solutions must not be applied when devices and/or packages are directly exposed to spray mists.
4. The need for initial application and frequency of reapplication can only be established through routine electrostatic field measurements during normal operations using an electrostatic field meter.

## Antistatic Floor Mats

The floor mat works with the heel strap/ESD shoes to provide a ground path for the dissipation of electrostatic charge, further reducing the charge accumulation on the personnel. In addition to dissipating charges, the floor mat also reduces triboelectric charging. The use of a floor mat is especially important in areas where increased personnel mobility is necessary. In addition, a floor mat can minimize charge accumulation on chairs, carts, and other objects that move across the floor.

## Identification

All static control programs must have appropriate symbols to identify static sensitive devices and assemblies. All eX/SX-A/RTSX-S/RTSX-SU devices are shipped with an ESD sensitivity sticker to identify the devices as ESD sensitive. The sticker was created based on the ESD Association Standard ANSI ESD S8.1-1993.



### Notes:

1. Label size: 70x45
2. Corner radius: 2.5
3. "Warning" font: Arial Black 6
4. "Class Zero..." font: Arial 2.5
5. "Open..." font: Arial 1.5

Figure 5 • ESD Label

## Board-Level Considerations

Once the devices are installed onto board assemblies, the presence of decoupling capacitors or other circuit protection will reduce the ESD sensitivity. However, the following guidelines must be adhered to in order to further reduce the possibility of an ESD event:

- Follow standard analog layout techniques, placing all bypass and bulk capacitors as close to the devices as possible.
- Include a ground and power plane on the Printed Wire Board (PWB) / Printed Circuit Board (PCB).
- Keep the loop area between power and ground as short as possible.
- Keep the ESD sensitive devices away from the edges of the board and away from external wires, connectors, and power.
- Minimize trace inductance and capacitance.

## Conclusion

Actel eX, SX-A, RTSX-S, RTSX-SU devices are sensitive to ESD events above 75 V. However, the probability of an ESD event actually causing damage is low, since the sensitivity is limited to only four pins on each device. The probability can be further reduced by following the handling suggestions outlined in this application note.

## Export Administration Regulations (EAR)

The product described in this datasheet is subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

## List of Changes

Previous Version	Changes in Current Version 51900099-1/9.05*	Page
51900099-0/7.05	The "eX, SX-A, RTSX-S, and RTSX-SU ESD Test Results" was updated.	3

**Note:** \* The part number is located on the last page of the document.

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